Digital Filtering  
Project 2 : IIR  
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Executive Summary:

A sinusoid of 6kHz frequency has to be detected in a sensor application for which we wish to design and analyze possible narrowband IIR filters. Of the possible designs, elliptic filter is chosen for further study and analysis. Direct II and Cascade architectures are considered and analyzed in further detail in terms of their immunity to finite word length effects. A sampling rate of 44.1kHz is used and a *Bilinear Z-Transform* is used as the specifications are in the frequency domain.

Problem Statement:

A sinusoid of 6kHz frequency is transmitted by a sensor which needs to communicate. Our job is to design a narrowband IIR filter to filter this signal reliably (for further detection possibly). The sampling rate to be used 44.1kHz. A -1.5dB of passband error and -40dB of stopband error is allowed.

Part I: IIR Design

1.1 The four filters, Butterworth, Chebyshev I, Chebyshev II and Elliptic are designed for the given specifications. The center frequency is 6000Hz. Maximum passband error was found to be around -15dB within the passband edges i.e. between [4800,5200]Hz. However error within stopband edges [4500, 5500]Hz is found to be -1.5dB at the stopband edges. The following table summarizes the 4 designs and figure 1 shows the magnitude response of the four filters. As expected ripple can be seen in Chebyshev I and elliptic filters. Pole-zero plot of the four filters is shown in figure 2.

Filter Design Comparison

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Filter | Order | Max. passband error (dB) | Max. lower stopband error (dB) | Max. upper stopband error (dB) |
| Butterworth | 12 | -10.8 | -49.29 | -46.56 |
| Chebyshev I | 8 | -15.99 | -45.68 | -43.70 |
| Chebyshev II | 8 | -19.82 | -40 | -40 |
| Elliptic | 6 | -15.99 | -40 | -40 |

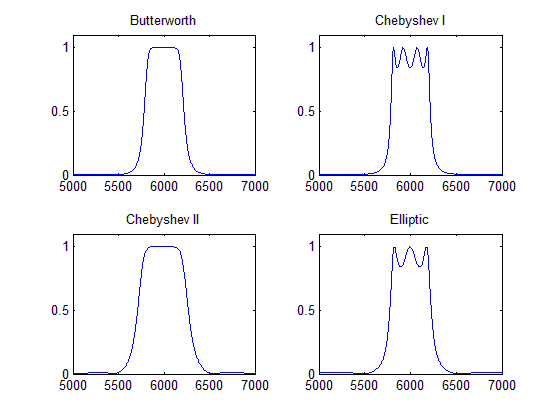


Figure 1: Magnitude frequency response of the four filters

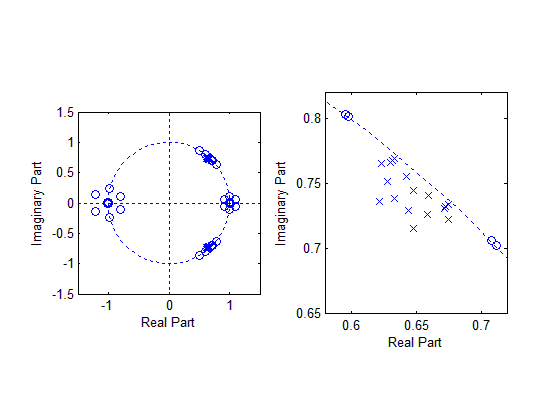
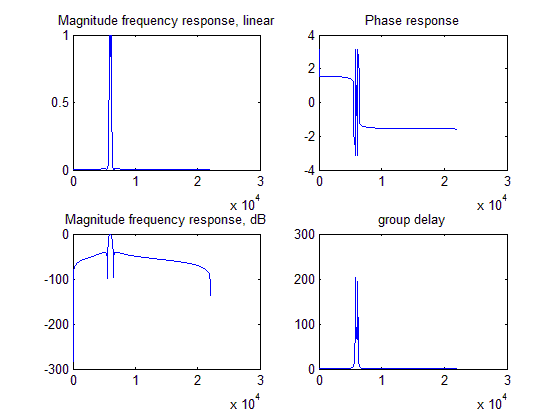


Figure 2: Pole zero plot of the four filters.

1.2 As the elliptic filter designed above has an order of 6, the filter is retained for further study. The magnitude frequency response in linear and dB scale along with phase and group delay are plotted in figure 3. 

1.3 A 15% emphasis is given to the lower passband by adjusting the magnitude of the pole at the lowest frequency. The magnitude is increased by a factor of 1.00065. If not careful the pole can go out of the unit circle.

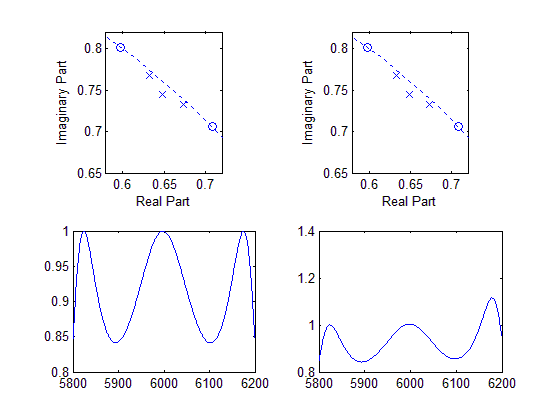


Figure 4: Pre-emphasis of 15% on lower passband

1.4 Figure 5 shows the 4 SNR cases of *inf,* 10dB, 0dB and -10dB. As expected the noise level increases as the SNR decreases. The filter cuts off out of band noise which can be seen by the absence of the red noise floor.

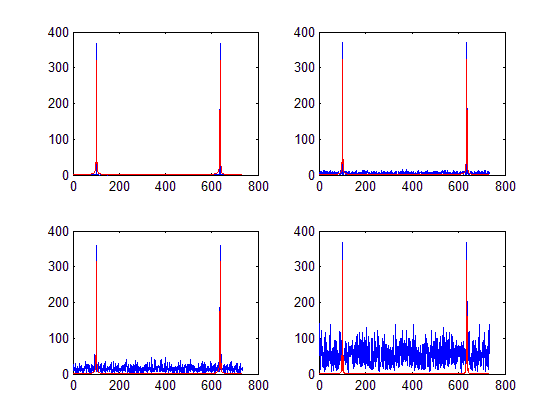


Figure 5: inf, 10, 0, -10dB SNR test cases.

Part II: IIR Architecture

2.1 MATLAB’s convention for state representation is followed to avoid confusion.

Direct II state matrices:

A\_d2 =

3.9068 -8.0391 9.8976 -7.9131 3.7853 -0.9537

1.0000 0 0 0 0 0

0 1.0000 0 0 0 0

0 0 1.0000 0 0 0

0 0 0 1.0000 0 0

0 0 0 0 1.0000 0

B\_d2’ =

1 0 0 0 0 0

C\_d2 =

0.0023 -0.0096 0.0177 -0.0190 0.0115 -0.0035

D\_d2 =

0.0018

Cascade state matrices are:

|  |  |  |
| --- | --- | --- |
| A\_c(:,:,1) =  1.2966 -0.9748  1.0000 0 | A\_c(:,:,2) =  1.2642 -0.9889  1.0000 0 | A\_c(:,:,3) =  1.3459 -0.9894  1.0000 0 |
| B\_c(:,:,1) =  1  0 | B\_c(:,:,2) =  1  0 | B\_c(:,:,3) =  1  0 |
| C\_c(:,:,1) =  0.0023 -0.0035 | C\_c(:,:,2) =  0.0683 0.0111 | C\_c(:,:,3) =  -0.0706 0.0106 |
| D\_c(:,:,1) =  0.0018 | D\_c(:,:,2) =  1 | D\_c(:,:,3) =  1 |

As the filter order is 6, there are 3 SOS (second order sections). A gain 0.0018 is incorporated into the D matrix of the first section.

2.2 The following table summarizes the findings on the two architectures.

|  |  |  |  |
| --- | --- | --- | --- |
| Architecture\coefficient | |Largest| | |Smallest| | #of nonzero, non-unity coefficients |
| Direct II | 9.897619 | 1.790617e-003 | 13 |
| Cascade | 1.345945e+000 | 1.790617e-003 | 13 |

As sample rate is low and floating point precision an be used (assuming a 32bit representation), both the two architectures will perform the same. Hence there is no significant design choice. However the largest coefficient in Cascade architecture is 1.35 where as in Direct II it is 9.89. which means Direct II needs 2 more bits over Cascade to represent the coefficients.

Part III: IIR Test and Evaluation.

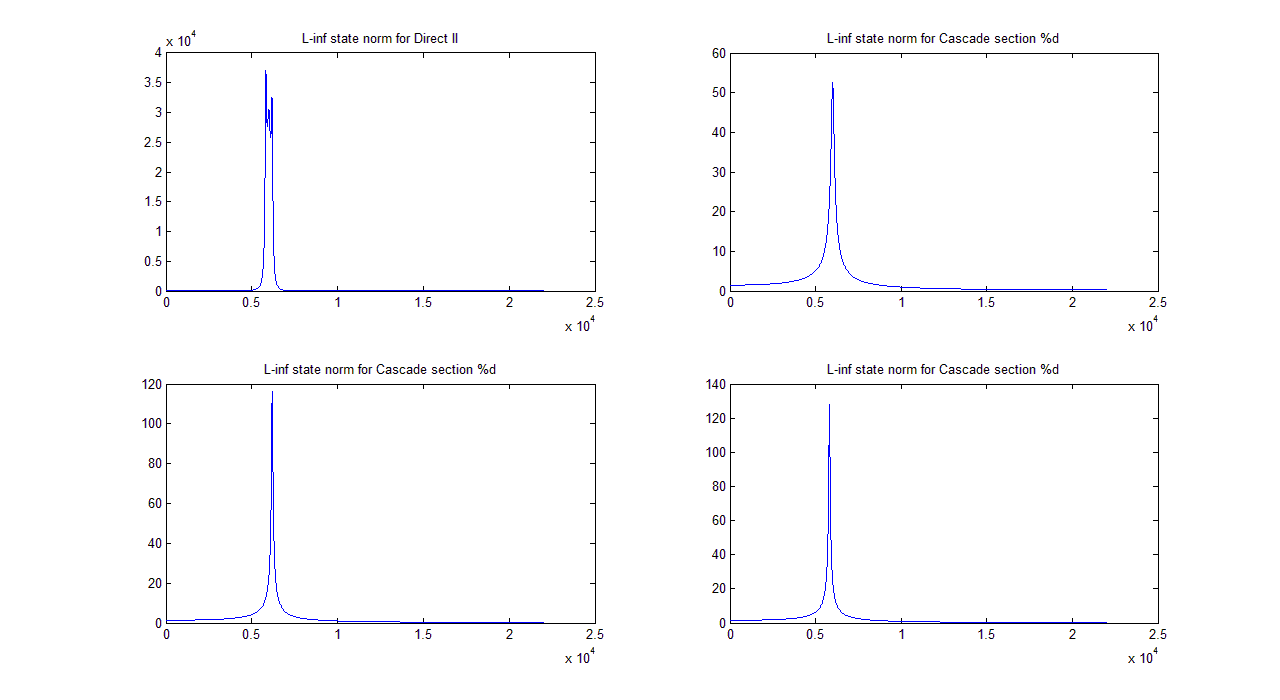
3.1 To calculate the L2 state norm, the Lyapunov Matrix is evaluated recursively.

3.2 For the Linf norm, the impulse response at each state is computed with a unit impulse at the input. For Direct II architecture, the L2 norms for all state are the same. For Cascade states within each section have the same norms.

3.3 L1 norms are computed from the impulse responses obtained earlier.

Table 4: Lp norms

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| L2 | x1 | x2 | x3 | x4 | x5 | x6 |
| Direct II | 4.311450e+003 | | | | | |
| Cascade | 5.942258e+000 | 5.942258e+000 | 8.707330e+000 | 8.707330e+000 | 9.343639e+000 | 9.343639e+000 |
| Linf | x1 | x2 | x3 | x4 | x5 | x6 |
| Direct II | 3.711263e+004 | | | | | |
| Cascade | 5.259709e+001 | 5.259709e+001 | 1.164070e+002 | 1.164070e+002 | 1.278996e+002 | 1.278996e+002 |
| L1 | x1 | x2 | x3 | x4 | x5 | x6 |
| Direct II | 6.333835e+004 | | | | | |
| Cascade | 6.694592e+001 | 6.694592e+001 | 1.482053e+002 | 1.482053e+002 | 1.628378e+002 | 1.628378e+002 |



3.4 The fractional bits are varied from F = 1:15 and the log2(error\_variance) is plotted on y-scale vs F on x-scale.

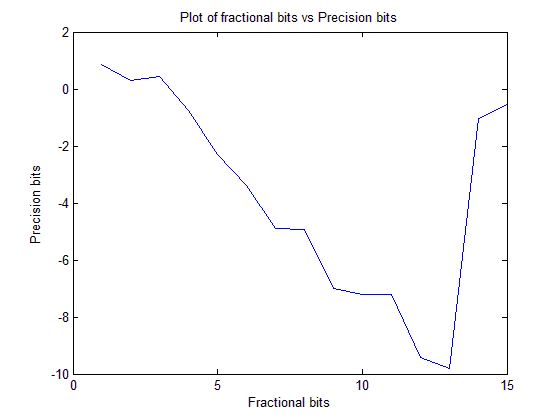


Figure 7: Precision bits vs Fractional bits

The plot in the above figure is for Cascade architecture. Among the range of values 1-15, F=13 seems to give the most precision bits. For Direct II architecture, overflows occurred for 96 times in the evaluation of states while 0 times for the evaluation of y, output.

3.5 L1 norm is 6 bits for Cascade section 1, which means that we need to devote 6 bits to integer bits. From the plot, 3 integer bits seem to do better for this input of 100 rands i.e., 100 uniformly distributed pseudo random numbers.

3.6 The 16 bit solution chosen is with 13 fractional bits of precision. Using SNRs of inf, 10,0,-10dB at the input resulted in output SNRs of Inf 27.8645 17.9835 7.6999dB.

3.7 There is an approximate delay of 120 samples for the output to catch up with the input. The error mean is -7.2313e-4 and error variance is -14.47 in bits. I have used 13 bits of fractional precision.

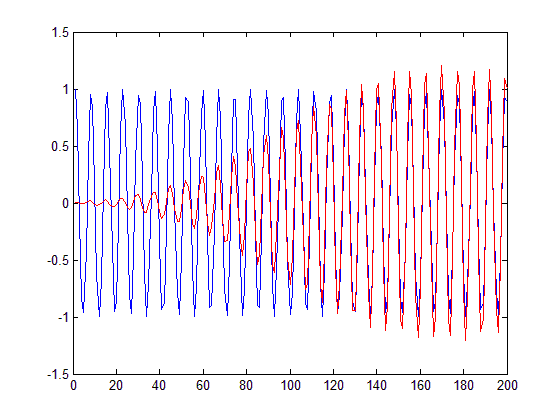


Figure 8: delay in sinusoid

Part IV: Applications

4.1 A delay of 130 samples can be seen in the output(red) to reach the full value.

50% 80

75% 120

95% 130

100% 130

The group delay vs frequency plot shows that the delay will be very high should the frequency of the sinusoid change a little bit

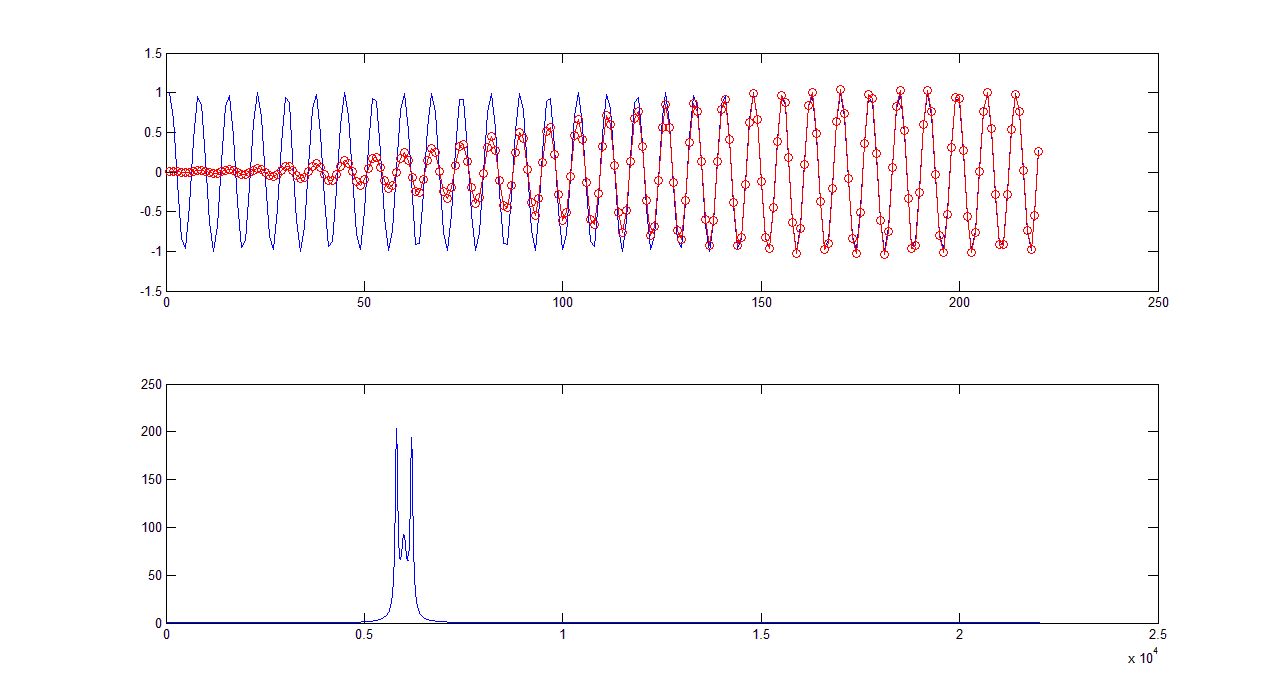


Figure 9: delay in sine(top), group delay(bottom)

4.2 For the Direct II architecture, there are 6 non-zero-unity in the c matrix and 6 in the A matrix. So a total of 12 coefficients need to be multiplied with the state vector.

If these two operations can happen parallel, then 6.25ns\*6 + 2\*6.25ns would require to complete a filter cycle. The second term is required for the data load operation. So a cycle time of 50ns can be expected.

If the above instructions cannot take place parallel, then (6.25ns\*6 + 6.25ns\*2)\*2 is required, i.e., 100ns per filter cycle.

4.3 The accumulator used in 3.4 doesn’t have extended precision. Hence the number of overflows would reduce drastically. Also the multipliers are 16x16 multipliers, hence in this case, we have more bits and hence more precision.

Conclusion:

The emphasis of this project on the architecture or the internal wiring diagram of the filter. As we have seen, different wiring diagrams can still maintain the output transfer function the same(floating point case) while having certain advantages and disadvantages. The filter removes out of band noise which is expected. Firstly we have seen that moving a pole closer to the unit circle results in an increase of the magnitude response of the filter at that frequency. Secondly the lack of extended precision in the accumulators results in a large number of overflows. This can also be seen from figure 7 where the error increases in a huge step once the integer bits are reduced further. The state norms also corroborate with this fact. The group delay of this filter is around 120 samples at 6kHz and increases at the edges to ~200samples. So should the input sinusoid be of a different frequency, it would result in a large delay. Finally the filter cycle is around 50ns or 100ns depending on the assumption stated on Part IV.